

THE "TOP-10 DESIGN KILLERS" DIAGNOSTIC

Why FPGAs Fail at 99% Completion

By Majid Kalsi, Principal Consultant | MKA Inc.

In 15 years of forensic FPGA analysis, we have found that the majority of "unexplainable" failures and timing closure bottlenecks are not caused by silicon errata, but by specific, repeatable architectural flaws.

At MKA Inc., our **48-Hour Rescue Audit** tests your design against these ten failure modes to identify the root cause of stalled production.

I. THE CLOCKING TRAPS

1. **Gated & Muxed Clocks** Using combinational logic on clock lines is inherently problematic. This practice introduces the risk of glitches on the output, which are dangerous when driving clock inputs.
2. **Clock Delay Chains** Designers often use delay chains to resolve clock skew issues. However, because routing delays vary across the die, this approach is unpredictable and statistically unreliable for production.
3. **Clock-as-Data** Using a clock signal as data is essentially a timing constraint issue. Many standard timing tools (like legacy ISE or TAN) will not automatically analyze these paths, leading to unconstrained and untested logic.

II. THE RESET HAZARDS

4. **Unsynchronized External Resets** An external reset that is not synchronized—or is incorrectly synchronized—to the destination clock domain is a primary cause of intermittent failure.
5. **Cross-Domain Internal Resets** A common error occurs when a reset generated in one clock domain is used directly in another asynchronous clock domain without re-synchronization.
6. **Combinatorial Logic on Resets** Placing combinational logic on a reset path creates a high risk of glitches. A glitch on a reset input is critical, as it can inadvertently clear state machines or registers during valid operation.

III. THE CROSS-DOMAIN (CDC) KILLERS

7. **Improper Synchronization** Signals crossing clock domains must follow strict synchronization rules to avoid metastability. Common violations include failing to use a minimum of two stages or placing logic between synchronization stages.
8. **The Nyquist Violation** Transferring a pulse from a fast clock domain to a slower clock domain often fails if the signal is not extended. Without pulse-width extension, the slower clock may miss the data capture entirely.
9. **Unsynchronized Bus Transfers** Attempting to synchronize multiple bits (a bus) using individual synchronizers causes data incoherency. Valid transfer methods (FIFO, Dual Port RAM, or Handshake Protocols) are required to prevent memory collisions and data corruption.

IV. THE "SILENT" KILLER

10. **Latches** Latches are fundamentally "not a good idea" in modern FPGA architectures. They create significant timing ambiguity and are often inferred unintentionally during synthesis.

STUCK IN THE LAB? "We don't know what we don't know." If your design works in simulation but fails in the real world, you are likely trapped in one of the categories above.

Contact MKA Inc. for a 48-Hour Forensic Audit.

Email: info@mka.solutions

Web: <https://hardwarebee.com/vendors/mka-inc>